Data Acquisition System

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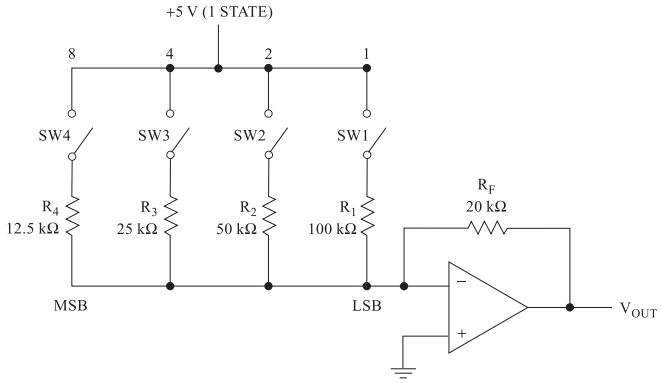
ME 361: Instrumentation & Measurement

Digital to Analog Conversion

DACs or D/A converters are used to convert digital signals representing binary numbers into proportional analog voltages.



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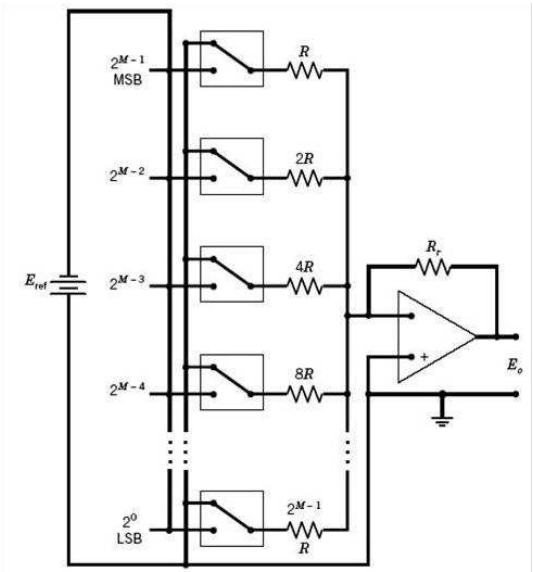
A 4-bit input Binary-weighted D/A converter

- A DAC converts a digital 'word' consisting of a number of bits into a voltage or current that represents the binary number value of the digital word.
- An 8-bit DAC, for example, may produce an output signal of 0 V when the binary word applied to its digital input is 00000000_2, and 2.55 V when the digital inputs see a word of 11111111_2.
- Similar to analog input configuration, a common DAC is shared among multiplexed output signals.
- Standard analog output ranges are essentially same as analog inputs: ±5 V dc, ±10 V dc, 0 - 10 V dc, and 4-20 mA dc.



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$$I = E_{ref} \sum_{M=1}^{N} \frac{c_m}{2^{m-1}R}$$

$$E_o = IR_r$$

$C_m = 0$ *or* 1: depending on the mth bit value of the register that controls the switch setting.

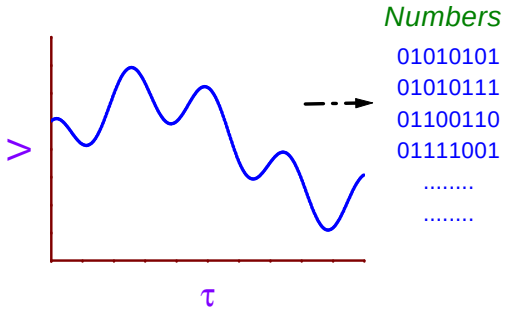
- The binary weighted resistor ladder suffers from a series drawback in actual practice. The values of input resistors tend to become very large and very small at the ends of the range as the bit length of the input word becomes larger.
- If R is set to 10 kΩ, then R_8 will be 1.28 MΩ. If we assume a reference potential E of 5.0 V, then I_8 will be only 3.9 μA which is too small to be resolved because of the noise problems.
- In commercial DACs, all the resistors have a value of either R or $2R$. The gain of the amplifier is unity, so E_o can be expressed as:

$$E_o = E \sum_{i=1}^{n} \frac{a_i}{2^i}$$

(provided that $R_L >> R$, so that the voltage divider effect between the ladder and R_L can be safely neglected).

Analog to Digital Conversion

- In A/D conversion process continuous electrical signals are converted to the digital language of computers.
- If a 8-bit ADC has a 0-to-2.55 V input signal range, then a 0 V input could produce an output word of 00000000_2, while the +2.55 V level seen at the input would produce an output word of 11111111_2.



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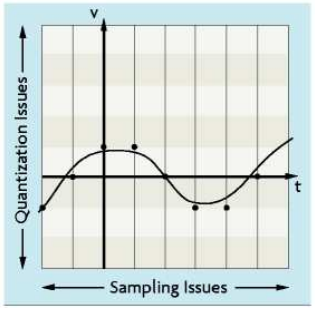
A/D Conversion Compromises



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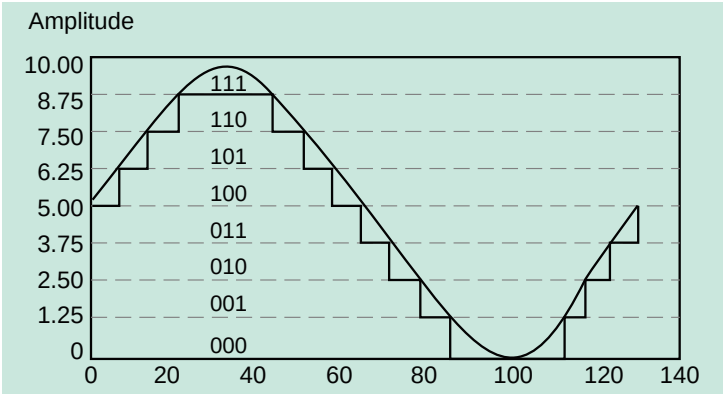
A/D conversion processes pose **two** primary challenges:

1. **Quantization** - refers to uncertainty introduced upon conversion of an analog voltage to a digital number.
2. **Sampling** - refers to acquiring data only at discrete intervals, with no informations in between.

Analog to Digital Conversion



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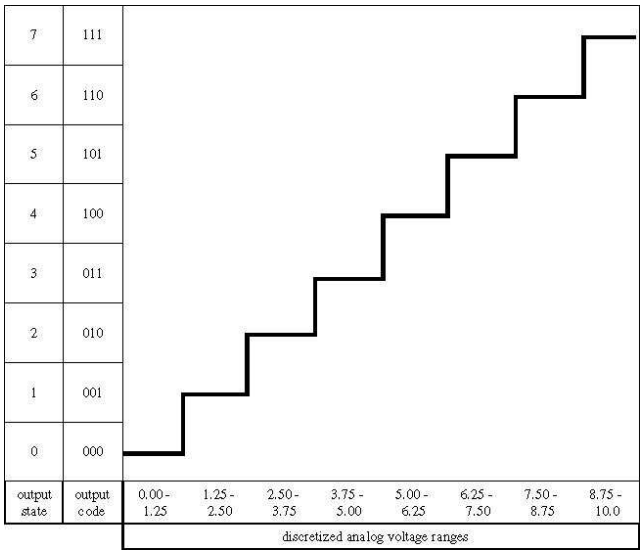
Digitized Sine Wave with a Hypothetical 3-Bit ADC



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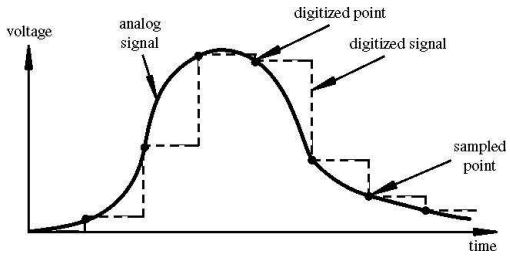
Resolution & Quantization

- *Resolution* refers to the smallest signal that can be detected by a measurement system. It can be expressed in bits, in proportions, on in percentage of full scale.
  $Resolution \equiv Q = \frac{E_{\text{Full Scale}}}{2^{\text{Number of Bits}}}$
- A system may have 12-bit resolution, one part in 4096 resolution, and 0.0244% of full scale.
- *Quantization error* is the inherent uncertainty in an A/D conversion due to the finite resolution of the system.
- An 8-bit ADC with E_{FS} of 10 V could detect a minimum of $10/256 = 0.0391$ V. The higher the resolution, the smaller the detectable voltage change.
- *How many bits are needed to obtain a resolution of 0.01%?*

Range of Values of Digital Quantities

No of bits	Number of States	Resolution (%)
1	$2^1 = 2$	50
2	$2^2 = 4$	25
3	$2^3 = 8$	12.5
4	$2^4 = 16$	6.25
8	$2^8 = 256$	0.391
10	$2^{10} = 1024$	0.098
12	$2^{12} = 4096$	0.024
16	$2^{16} = 65536$	0.001526
20	$2^{20} = 1048576$	0.000095

Analog Signal & Sampled Equivalent



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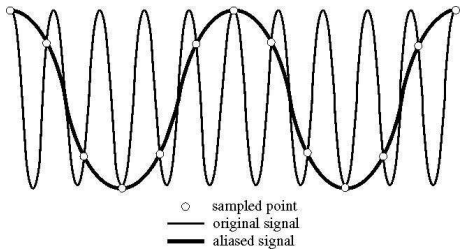

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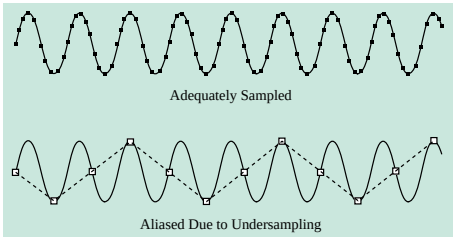
Shanon's Sampling Theorem

To faithfully represent the analog signal, sampling frequency f_s such that must be greater than Nyquist frequency, f_N:

$$f_s > f_N \equiv 2f_{max}$$

- Time interval between the digital samples is $\Delta t = 1/f_s$
- If $f_s < f_N$, *aliasing* can result and totally non-existent frequencies may be indicated.



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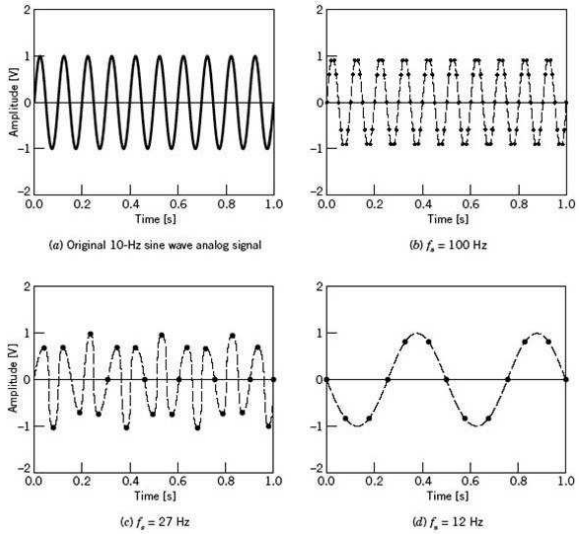
Example: Effect of Sampling Rate



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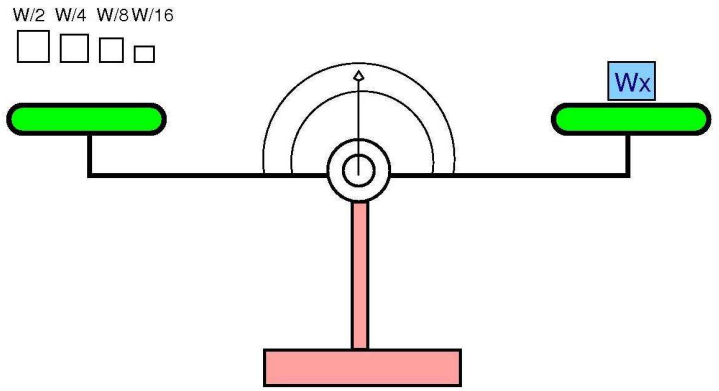
Types of A/D Converters

1. Successive Approximation (SA) ADC
2. Flash/Parallel ADC
3. Dual-slope Integrating ADC
4. Servo/Binary-counter/Ramp ADC

Type	Speed	Resolution	Noise Immunity	Cost
1.	Medium	10-16 bits	Poor	Low
2.	Fast	4-8 bits	None	High
3.	Slow	12-18 bits	Good	Low
4.	Slow	14-24 bits	Good	Medium

Successive Approximation ADC



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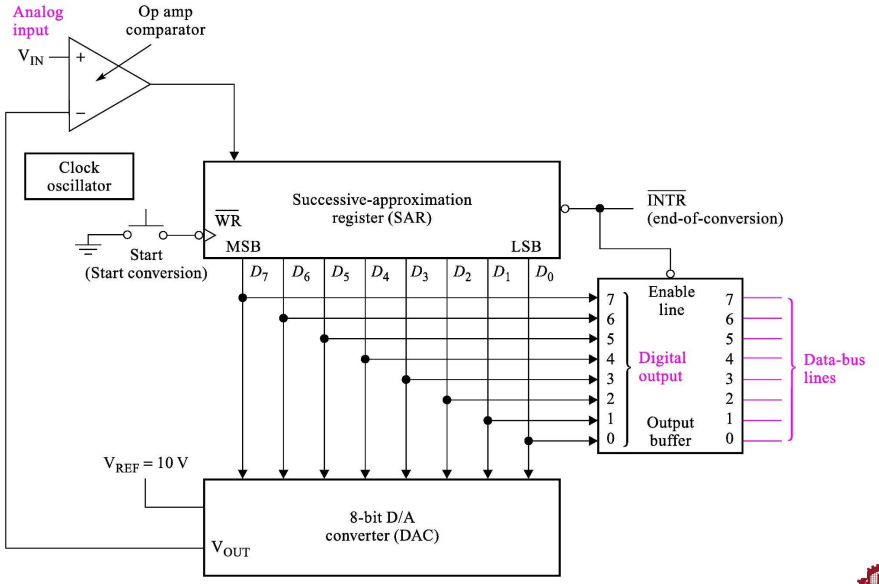

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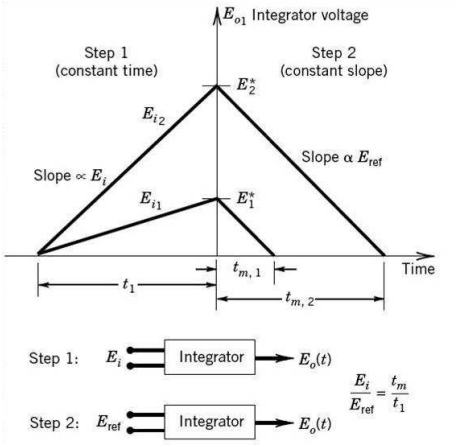
- A SA register(SAR) contains the control logic, a shift register, and a set of output latches, one for each register section. The outputs of the latches drive a DAC.
- A start pulse sets D7 (first bit of the shift register, MSB) *high*. DAC sees the word 10000000_2 & generates the output voltage, $V_{out} = 1/2E_{FS}$. If $V_{IN} > V_{out}$, then the D7 latch is set *high*, else it is set *low*.
- On the next clock pulse, D6 latch is set *high*. The process is continued through to LSB. If, on any trial, it is found that $V_{IN} < V_{out}$, then the corresponding bit is reset *low*. The process is continued until the voltages match within the least significant bit.

Dual-slope Integrating ADC



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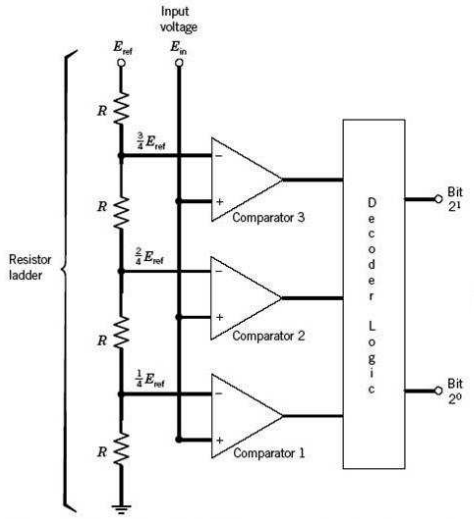
Output represents the integral or average of an input voltage over a fixed period of time. Hence, it smooths out signal noise.

Parallel or Flash ADC



Logic Scheme of a 2-Bit Parallel A/D Converter

Comparator States			Binary Output
HIGH	HIGH	HIGH	11
LOW	HIGH	HIGH	10
LOW	LOW	HIGH	01
LOW	LOW	LOW	00

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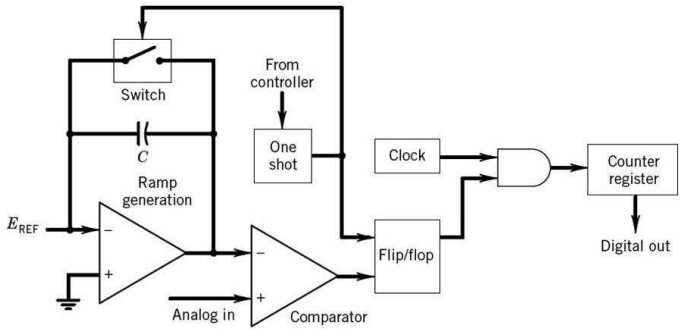
Ramp ADC



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E_{ref}, initially at zero, is increased at a set time steps & the ramp level is compared with the input voltage. The comparison is continued until the two are equal. The comparator output then goes to zero. It flips a flip-flop and the register count value will then indicate the digital binary equivalent of the input voltage.

ADC Speed Parameters

1. **Acquisition:** is the time required by the front-end analog circuitry to acquire a signal. Also called aperture time, it is the time for which the converter must see the analog voltage in order to complete a conversion.
2. **Conversion:** is the time needed to produce a digital value corresponding to the analog value.
3. **Transfer:** is the time needed to send the digital value to the host computer's memory.

Throughput, then, equals the number of channels being served divided by the time required to do all three functions.